REMARKS

Claims 1-27 and 29-66 are all the claims pending in the application.

Support for the amendment to claim 25 may be found in the specification as originally filed, for example, in the originally filed claims, Example 23 and page 56, line 32 to page 57, line 4 of the specification. Support for new claims 64-66 may be found in the specification as originally filed, for example, at page 57, lines 19-21, page 58, lines 29 to 33, in original claim 36.

I. The Rejection under 35 U.S.C. §112

Claims 25-32 are rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite.

Claim 25 is amended to clarify the constitution of the multilayer printed circuit board according to the present invention. Claim 25 is amended to clarify that the resin insulating layers cover both sides of the resin substrate board and are comprised of the same resin material, and that a conductor circuit is built on each of the resin insulating layers and therefore on each side of the substrate.

II. The Rejection under 35 U.S.C. §102(e) Based on Oodaira et al

Claims 25-32 are rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Oodaira et al.

Applicants respectfully submit that the present invention is not anticipated by or obvious over the disclosures of Oodaira et al and request that the Examiner reconsider and withdraw this rejection in view of the following remarks.

Prior to addressing the Examiner's specific rejection, Applicants submit the following brief summary of the present invention. The summary of the invention is provided to the Examiner for the purposes of assisting the Examiner in understanding the claimed invention and the differences between the claimed invention and the cited art.

The present invention, as claimed in claim 25, recites "a multilayer printed circuit board comprising a resin substrate board carrying, on both sides thereof, resin insulating layers comprised of the same resin material and a conductor circuit on each of said resin insulating layers,

wherein said resin insulating layers comprise thermosetting polyolefin resin, or a mixed resin of a thermosetting resin containing at least one member selected from among thermosetting polyolefin resin, epoxy resin, polyimide resin, phenolic resin and bis (maleimide) triazine resin and a thermoplastic resin, and

said conductor circuit has been formed on the surfaces of said resin insulating layers by way of a metal layer composed of at least one metal selected from among metals (exclusive of Cu) of the 4th through 7th periods in Group 4A through Group 1B of the long-form periodic table of the elements, A1 and Sn."

In the multilayer printed circuit board according to the present invention, the metal layers have a high adhesion to the resins of the insulating layers (See Applicants' specification, page 54, lines 30 to 31). Therefore, even when warpage occurs in the resin substrate board, no delamination is induced between the resin insulating layer and the conductor circuit.

Further, since the resin insulating layers and the metal layers are arranged symmetrically on both sides of the resin substrate board, with the resin insulating layers comprising the same resin material, the amount of warp generated in the substrate board is reduced and cracking across the interface between the conductor circuit and the resin insulating layer under the conditions of the heat cycle test can be suppressed.

Moreover, by forming the above-mentioned metal layer, the resin insulating layer can obtain a firm adhesion to the conductor circuit without providing a roughened layer on the surface thereof. As a result, no signal conduction delay occurs even when high-frequency signals are used (see Applicants' specification, page 54, line 30 to page 55, line 2).

As claimed in claim 25, the resin insulating layers comprise thermosetting polyolefin resin, or a mixed resin of a thermosetting resin and a thermoplastic resin.

Resin insulating layers comprising the mixed resin is superior to resin insulating layers comprising a thermoplastic resin. In addition, since their fracture

rigidity is high, generation of cracks is suppressed (see Applicants' specification, page 57, lines 27 to 30).

Resin insulating layers comprising the thermosetting polyolefin resin are comparable to epoxy resin in heat resistance so that no striping of the conductor circuit occurs even at the solder melting temperature. In addition because of the high fracture rigidity, there is no risk for cracks originating from the interface between the conductor circuit and the resin insulating layer under the conditions of the heat cycle test (See Applicants' specification, page 57, lines 24 to 30). Resin insulating layers comprising the mixed resin also have such effects.

Turning to Oodaira et al, according to Oodaira et al, a thermoplastic resin is used to form resin substrates of a circuit board and the substrate and the circuit pattern are plastically deformed and bonded (Oodaira et al, claim 1). Oodaira et al takes advantage of thermoplastic resins which are softened and deformed when heated. This means thermoplastic resins having low heat resistance.

To the contrary, Applicants' claimed resin insulating layers comprise thermosetting polyolefin resin, or a mixed resin of a thermosetting resin and a thermoplastic resin (where the thermosetting resin contains at least one member selected from among thermosetting polyolefin resin, epoxy resin, polyimide resin, phenolic resin and bis (maleimide) triazine resin). In view of the material of the resin insulating layers, the multilayer printed circuit board is unexpectedly improved as discussed above, and the circuit board comprising a thermoplastic resin

according to Oodaira et al is inferior in heat resistance as compared to the multilayer printed circuit board according to the present invention.

Oodaira et al discloses resin substrates comprising a thermosetting resin (Oodaira et al, col. 3, lines 21 to 25), however Oodaira et al fails to teach or suggest to use thermosetting polyolefin resin. Therefore, one of ordinary skill in the art would not have expected Applicants' above-mentioned effects of resin insulating layers comprising thermosetting polyolefin resin.

Regarding the metal layer according to the present invention, preferably, it is formed by plating, PVD or CVD. See Applicants' new claim 64. Such techniques allow the formation of a uniform thin metal layer. Applicants respectfully submit that claim 64 is allowable for at least the reasons as claim 25 is allowable.

Oodaira et al discloses a circuit pattern of a conductive resin composition consisting of a synthetic resin binder and conductive material (Oodaira et al, col. 3, lines 10 to 13). However, Oodaira et al is silent about forming a metal layer on the surfaces of the resin substrate by plating, PVD or CVD. Further, Oodaira et al does not teach or suggest that a metal layer formed by such methods is thin and has a uniform thickness.

Accordingly, the circuit board according to Oodaira et al is different in constitution from the multilayer printed circuit board according to the present invention. Oodaira et al fails to teach or suggest resins as described in the present invention which show high adhesion to conductor circuits, and one cannot predict

the above-mentioned unexpected effects of resin insulating layers according to the present invention. Therefore, the present invention is not anticipated by and not obvious over Oodaira et al.

Further, since the independent claim 25 is not anticipated by and not obvious over Oodaira et al, Applicants respectfully submit that the rejection of the dependent claims 26, 27 and 29-32 is also overcome for at least the same reasons as discussed above.

For the above reasons, it is respectfully submitted that the subject matter of claims 25-32 and 64 is neither taught by nor made obvious from the disclosures of Oodaira et al and it is requested that the rejection under 35 U.S.C. §102(b) be reconsidered and withdrawn.

III. The Rejection under Based on Oodaira et al in view of Sera et al

Claim 30 is rejected under 35 U.S.C. §103(a) as allegedly being obvious over Oodaira et al in view of Sera et al.

Applicants respectfully submit that the present invention is not obvious over the disclosures of Oodaira et al and Sera et al and request that the Examiner reconsider and withdraw this rejection in view of the following remarks.

Sera et al discloses a flexible wiring board having a conductor circuit 82 with a metal layer 83 on its surface. The metal layer 83 has an interlayer resin insulating layer 84 as built thereon. However, Sera et al fails to teach that the

conductor circuit 82 is formed on the surfaces of the insulating film 81 by way of a metal layer. Therefore, the wiring board according to Sera et al is different in constitution from the multilayer printed circuit board according to the present invention.

According to the present invention, as mentioned above, the metal layer is formed to obtain a firm adhesion between the resin insulating layer and the conductor circuit, without providing a roughened layer on the surface of the resin insulating layer. Sera et al is silent about such an effect. The metal layer 83 is formed to obtain an excellent conductivity with reduced wiring resistance (Sera et al, col. 15, lines 44 to 48). Therefore, the effect of the metal layer according to the present invention is not described in and cannot be predicted from Sera et al.

Accordingly, claim 30 is not anticipated by and not obvious over Sera et al, and one cannot obtain the multilayer printed circuit board of the present invention from the combination of Oodaira et al and Sera et al.

For the above reasons, it is respectfully submitted that the subject matter of claim 30 is neither taught by nor made obvious from the disclosures of Oodaira et al and Sera et al and it is requested that the rejection under 35 U.S.C. §103(a) be reconsidered and withdrawn.

IV. The Rejection under 35 U.S.C. §103 Based on Oodaira et al

Claim 32 is rejected under 35 U.S.C. §103 as allegedly obvious over the disclosures of Oodaira et al.

Applicants respectfully submit that dependent claim 32 is not obvious over Oodaira et al for at least the same reasons as set forth above in Section II and it is requested that the rejection under 35 U.S.C. §103(a) be reconsidered and withdrawn.

V. The Rejection under 35 U.S.C. §103 Based on Oodaira et al in view of Nye, III et al

Claim 31 is rejected under 35 U.S.C. §103 as allegedly obvious over the disclosures of Oodaira et al in view of Nye, III et al.

Applicants respectfully submit that the present invention is not obvious over the disclosures of Oodaira et al in view of Nye, III et al and request that the Examiner reconsider and withdraw this rejection in view of the following remarks.

Nye, III et al is related to a semiconductor chip 30 with a solder layer 120 deposited thereon. Nye, III et al does not disclose a multilayer printed circuit board. Therefore, the present invention is not anticipated by and not obvious over Nye, III et al.

Further, since claim 25 is not anticipated by and not obvious over Oodaira et al for the reasons as set forth in Section II above, dependent claim 31 is not obvious

over Oodaira et al in view of Nye, III et al. That is, the disclosures of Nye, III et al do not overcome the deficiencies in Oodaira et al discussed above.

For the above reasons, it is respectfully submitted that the subject matter of claims 31 is neither taught by nor made obvious from the disclosures of Oodaira et al in view of Nye, III et al and it is requested that the rejection under 35 U.S.C. §103(a) be reconsidered and withdrawn.

VI. Conclusion

In view of the above, Applicants respectfully submit that their claimed invention is allowable and ask that the rejection under 35 U.S.C. §112, the rejection under 35 U.S.C. §102 and the rejections under 35 U.S.C. §103 be reconsidered and withdrawn. Applicants respectfully submit that this case is in condition for allowance and allowance is respectfully solicited.

If any points remain at issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the local exchange number listed below.

Applicants hereby petition for any extension of time which may be required to maintain the pendency of this case.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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APPENDIX
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

Claim 28 is canceled.

25 (Amended). A multilayer printed circuit board comprising a resin substrate board carrying, [a resin insulating layer] on both sides thereof, resin insulating layers comprised of the same resin material and a conductor circuit built on each of said resin insulating [layer] layers,

wherein said resin insulating layers comprise thermosetting polyolefin resin, or a mixed resin of a thermosetting resin containing at least one member selected from among thermosetting polyolefin resin, epoxy resin, polyimide resin, phenolic resin and bis (maleimide) triazine resin, and a thermoplastic resin, and

each of said conductor [circuit has been] circuits are formed on the [surface] surfaces of said resin insulating [layer] layers by way of a metal layer composed of at least one metal selected from among metals (exclusive of Cu) of the 4th through 7th periods in Group 4A through Group 1B of the long-form periodic table of the elements, Al and Sn.

26 (amended). The multilayer printed circuit board according to Claim 25 wherein each of said metal [layer] layers is a layer containing at least one metal selected from among Al, Fe, W, Mo, Sn, Ni, Co, Cr, Ti and noble metals.

27 (amended). The multilayer printed circuit board according to Claim 25 wherein each of said resin insulating [layer] layers has a flat and level surface.

29 (amended). The multilayer printed circuit board according to Claim 25 wherein each of said resin insulating [layer] layers has a surface obtained by plasma treatment or corona discharge treatment.

30 (amended). The multilayer printed circuit board according to Claim 25 wherein each of said conductor [circuit] circuits has a metal layer composed of at least one metal selected from among metals (exclusive of Cu) of the 4th through 7th periods in Group 4A through Group 1B of the long-form periodic table of the elements, Al and Sn on its surface and said metal layer on the surface of said conductor circuits has an interlayer resin insulating layer or a solder resist layer [as] built thereon.

31 (amended). The multilayer printed circuit board according to Claim 25 wherein each of said metal [layer] layers built on the surface of said resin insulating [layer] layers has a Cu layer formed on its surface and said Cu layer has a conductor circuit constructed thereon.

32 (amended). The multilayer printed circuit board according to Claim 25 wherein the thickness of each of said metal [layer] layers is 0.01 to 0.2 μm.

New claims 64-66 are added.